DYNAMIC PHASE-LOCKED LOOP CIRCUITS AND METHODS OF OPERATION THEREOF

ABSTRACT OF THE DISCLOSURE

A phase locked loop (PLL) circuit includes a controlled oscillator circuit that is operative to generate an output clock signal responsive to an oscillator control signal according to a plurality of selectable transfer functions, and an oscillator control signal generator circuit that is operative to generate the oscillator control signal responsive to the output clock signal and a reference clock signal. The PLL circuit further includes a transfer function control circuit operative to transition operation of the controlled oscillator from a first one of the transfer functions to a second one of the transfer functions responsive to the oscillator control signal. For example, the transfer function control circuit may step the controlled oscillator circuit through a succession of the transfer functions in response to a change in a frequency of the reference clock signal and may enable a closed loop including the oscillator control signal generator circuit and the controlled oscillator circuit upon selection of each of the succession of transfer functions.